| REV | DESCRIPTION | ISSUE DATE |
|---|---|---|
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |

# S9501 Series BMC Card


| | |
|---|---|
| 01 | TABLE OF CONTENTS |
| 02 | DESIGN CHANGE HISTORY |
| 03 | BMC_260P_CONNERCTOR |
| 04 | SYSTEM BLOCK DIAGRAM |
| 05 | BMC_AST2600_PCIe &LPC &DDR4 |
| 06 | BMC_AST2600_SPI&UART&RGMII |
| 07 | BMC_AST2600_USB&JTAG&TAC |
| 08 | BMC_AST2600_PWR |
| 09 | BMC_AST2600_GND |
| 10 | BMC_AST2600_STRAPPING&ADC |
| 11 | TPM & Console header |
| 12 | PWM& FRU |
| 13 | Board ID& Thermal  Sensor |
| 14 | BMC_RESET&3V3_RGM&12Vto 3V3 |
| 15 | BMC_PWR SEQUENCE |
| 16 | 3V3 to 1V0_BMC/0.9A_MP2161 |
| 17 | 3V3 to 1V2/2V5_BMC/0V6/0.9A |
| 18 | 3V3 to 1V8_BMC/0.3A_NCP59748 |
| 19 | |
| 20 | |
| 21 | |
| 22 | |
| 23 | |
| 24 | |
| 25 | |
| 26 | |
| 27 | |
| 28 | |


## *TABLE OF CONTENTS*

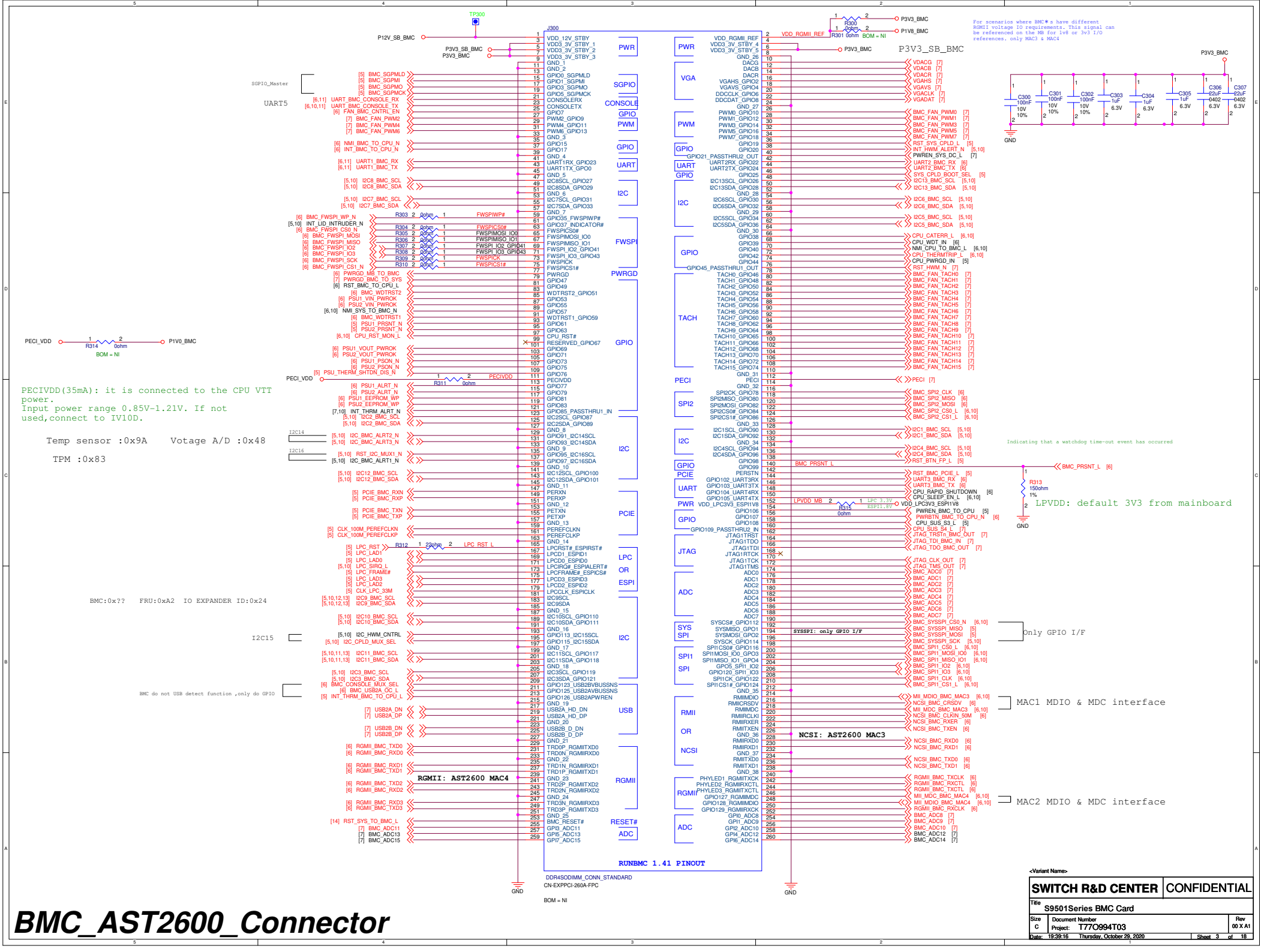
<Variant Name>

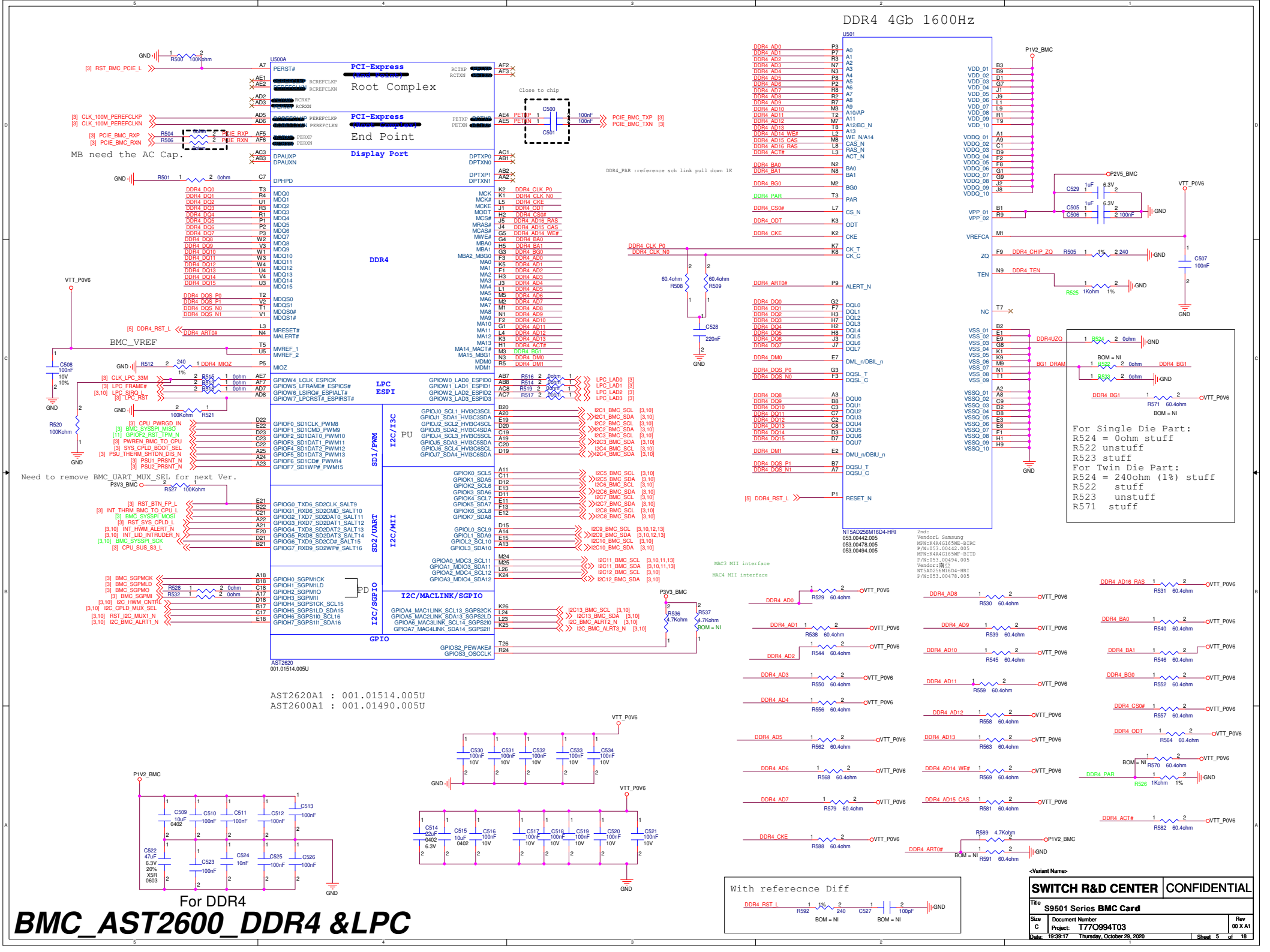
| | |
|---|---|
| **SWITCH R&D CENTER** | CONFIDENTIAL |

Title: S9501 Series BMC Card

Size: C | Document Number | Project: T77O994T03 | Rev: 00 X A1

Date: 19:39:16 Thursday, October 29, 2020 | Sheet 1 of 18


J300
RUNBMC 1.41 PINOUT
DDR4SODIMM_CONN_STANDARD
CN-EXPPCI-260A-FPC
BOM = NI
PECIVDD(35mA): it is connected to the CPU VTT power.
Input power range 0.85V~1.21V. If not used,connect to IV10D.
Temp sensor :0x9A Votage A/D :0x48
TPM :0x83
BMC:0x?? FRU:0xA2 IO EXPANDER ID:0x24
UART5
I2C15
RGMII: AST2600 MAC4
NCSI: AST2600 MAC3
P3V3_SB_BMC
LPVDD: default 3V3 from mainboard
Only GPIO I/F
MAC1 MDIO & MDC interface
MAC2 MDIO & MDC interface
SWITCH R&D CENTER
CONFIDENTIAL
S9501Series BMC Card
T77O994T03
Thursday, October 29, 2020
BMC_AST2600_Connector


DDR4 4Gb 1600Hz
U500A
PCI-Express
Root Complex
PCI-Express
End Point
Display Port
DDR4
LPC
ESPI
I2C/I3C
SD1/PWM
I2C/MII
SD2/UART
I2C/SGPIO
I2C/MACLINK/SGPIO
GPIO
AST2620
001.01514.005U
U501
NT5AD256M16D4-HRI
053.00442.005
053.00478.005
053.00494.005
MB need the AC Cap.
DDR4_PAR :reference sch link pull down 1K
Close to chip
BMC_VREF
Need to remove BMC_UART_MUX_SEL for next Ver.
MAC3 MII interface
MAC4 MII interface
AST2620A1 : 001.01514.005U
AST2600A1 : 001.01490.005U
For DDR4
With refereecnce Diff
For Single Die Part:
R524 = 0ohm stuff
R522 unstuff
R523 stuff
For Twin Die Part:
R524 = 240ohm (1%) stuff
R522 stuff
R523 unstuff
R571 stuff
SWITCH R&D CENTER
CONFIDENTIAL
S9501 Series BMC Card
BMC_AST2600_DDR4 &LPC
Document Number
Project: T77O994T03
Rev 00 X A1
Date: 19:39:17 Thursday, October 29, 2020
Sheet 5 of 18

To disable the CPU running, short FWSPICS0# to GND before SRST# reset completed

SPI1ABR# set to LOW for primary code

For SPI1ABR (PinAD10), it is used for selecting alternate boot source.
When this pin statis is LOW, it will force boot from primary code.
When this pin statis is HIGH, it will force to boot from alternate code.

remove INT_TSEN_NMI_N for next Ver.

PIN_A15 BMCINT function
remove at design Guide
Ver0.8

MAC1 & MAC2 is 1.8V I/O only, please note it did not support NCSI
3.3V I/O application.

RGMII 125MHz can be generated internally. When use internal source, this pin can be NC

NCSI :If the maximum trace length between AST2600 to the PHY is less than 10 inches, it could use AST2600 internal 50MHz clock output.

Don't use external 125MHz reference clock mode for RGMIICK pin, this function is used for debug purpose only. Please use internal PLL to generate RGMII or RMII reference clcok.

H24 :When used as RMII/NCSI 50MHz reference clock output, this pin should be connected to RMII1RCLKI and PHY RCLK input.

R1021 with R639 at FWSPIWP#

U602, U603 change 512Mb 065.00758.005 W25M512JVEIQ / MX25L51245GZ2I-08G

1st SPI flash 512Mb

2nd SPI flash 512Mb

BMC_FWSPI_MISO has pull high R 1017

Remove Flash Socket

Remove Flash Socket

<Variant Name>

| SWITCH R&D CENTER | CONFIDENTIAL |
|---|---|
| Title: S9501 Series BMC Card | |
| Size: C | Document Number: T77O994T03 | Rev: 00 X A1 |
| Date: 19:39:17 Thursday, October 29, 2020 | Sheet 6 of 18 |

Z0=50 ohm
2ND ORDER PI-FILTER put on MB

ADC8 ~ ADC15 Main GPIO Use

U500D
AST2620
001.01514.005U

MISC
FAN / THRU
DAC
USB
ADC
PECI
JTAG MASTER
JTAG SLAVE
CHASSIS INTRUSION

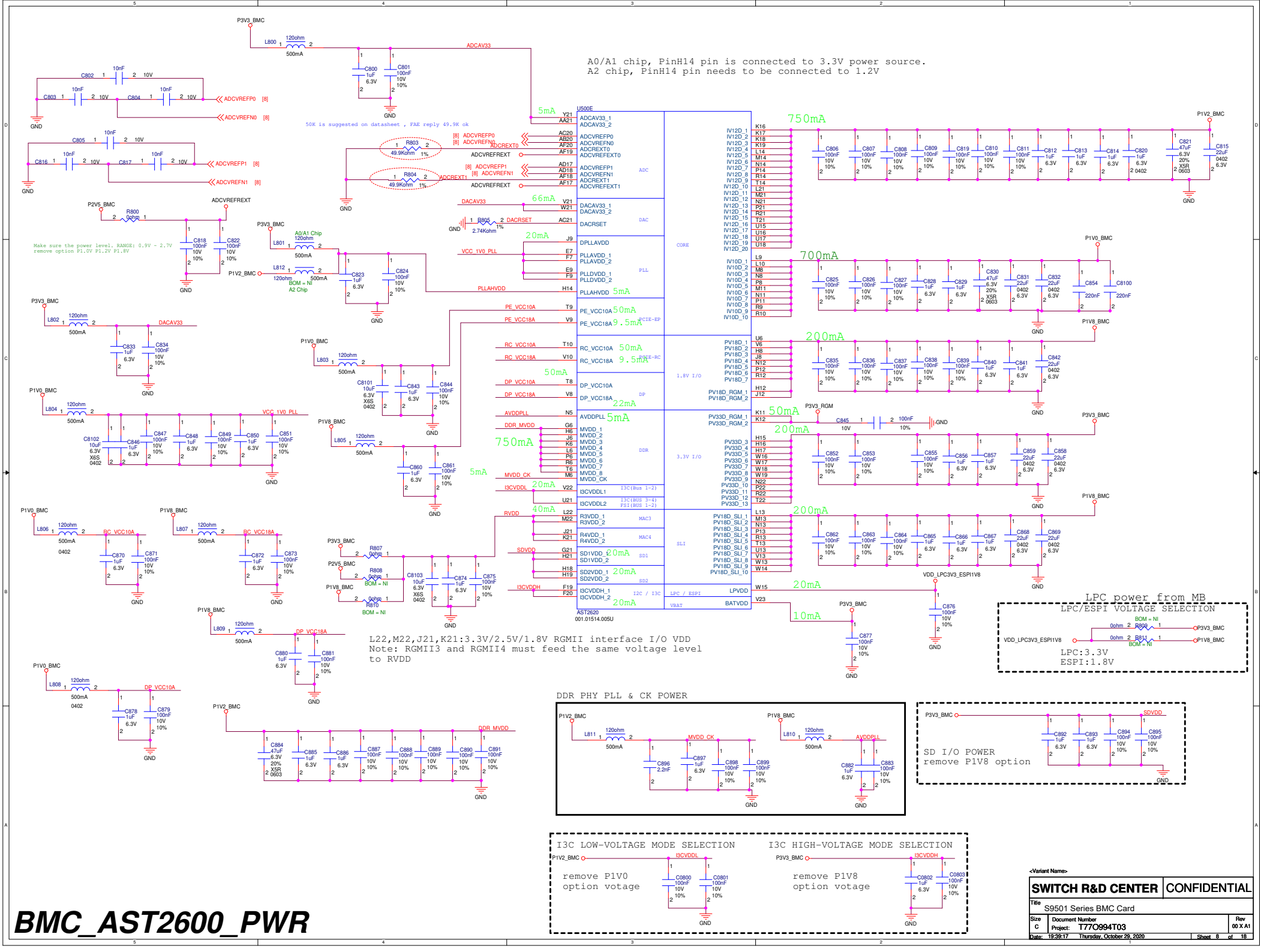
<Variant Name>

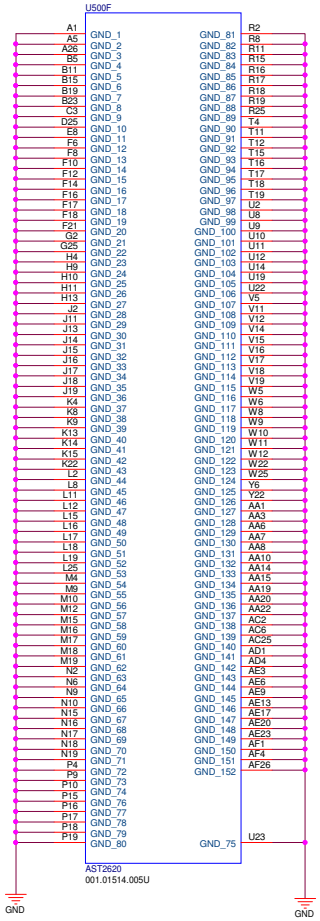
SWITCH R&D CENTER | CONFIDENTIAL

Title: S9501 Series BMC Card

Size: C | Document Number: T77O994T03 | Rev: 00 X A1

Date: 19:39:16 Thursday, October 29, 2020 | Sheet 7 of 18


A0/A1 chip, PinH14 pin is connected to 3.3V power source.
A2 chip, PinH14 pin needs to be connected to 1.2V
50K is suggested on datasheet , FAE reply 49.9K ok
Make sure the power level. RANGE: 0.9V ~ 2.7V
remove option P1.0V P1.2V P1.8V
L22,M22,J21,K21:3.3V/2.5V/1.8V RGMII interface I/O VDD
Note: RGMII3 and RGMII4 must feed the same voltage level
to RVDD
LPC power from MB
LPC/ESPI VOLTAGE SELECTION
LPC:3.3V
ESPI:1.8V
DDR PHY PLL & CK POWER
SD I/O POWER
remove P1V8 option
I3C LOW-VOLTAGE MODE SELECTION
remove P1V0
option votage
I3C HIGH-VOLTAGE MODE SELECTION
remove P1V8
option votage
BMC_AST2600_PWR
SWITCH R&D CENTER
CONFIDENTIAL
S9501 Series BMC Card
T77O994T03
00 X A1
Thursday, October 29, 2020
Sheet 8 of 18




<Variant Name>

| SWITCH R&D CENTER | CONFIDENTIAL |
|---|---|
| Title: S9501 Series BMC Card | |
| Size: C | Document Number / Project: T77O994T03 — Rev: 00 X A1 |
| Date: 19:39:16 Thursday, October 29, 2020 | Sheet 9 of 18 |

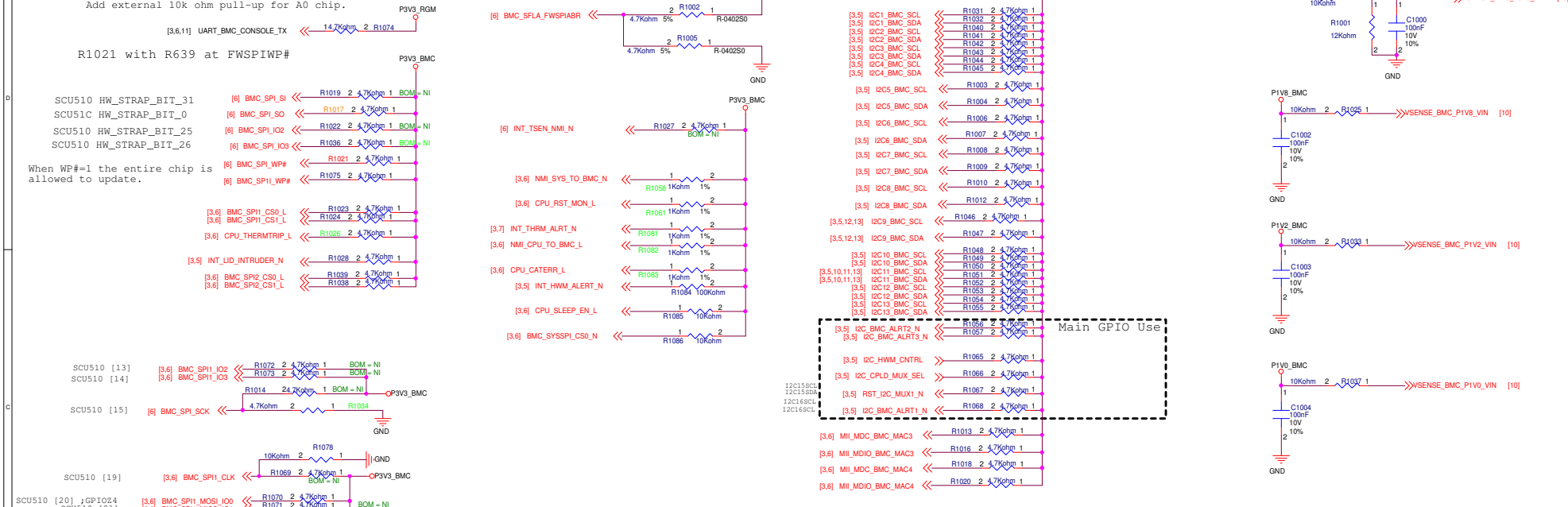
SCU500_HW_STRAP_BIT_0
Disable ARM CA7 CPU boot (TXD5)
0: Enable ARM CA7 CPU boot (default)
1: Disable ARM CA7 CPU boot
Add external 10k ohm pull-up for A0 chip.

The hardware strap pin 'FWSPIMISO' (BMC_SPI_SO) is used to enable the debug UART ports by controlling the default value loaded to these registers When this strap is set high

R1021 with R639 at FWSPIWP#

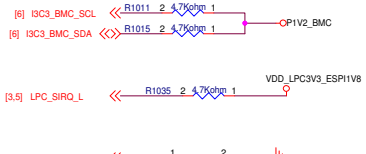
SCU510 HW_STRAP_BIT_31
SCU51C HW_STRAP_BIT_0
SCU510 HW_STRAP_BIT_25
SCU510 HW_STRAP_BIT_26

When WP#=1 the entire chip is allowed to update.

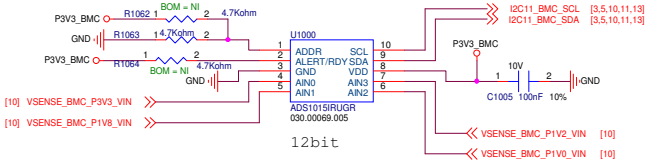



When SCU510[30]=0 (Default) <--SW setting , see datasheet page 456
(1.)Enable LPC mode (OTPSTRAP[38])
0: eSPI mode (default)
1: LPC mode <---setting
(2) Enable Boot from Uart5 by Pin Strap (OTPSTRAP[40])
0: Disable(default)
1: Enable boot from Uart5
(3)Enable Secure Boot by Pin Strap (FWSPIMOSI) <--HW setting
0: Disable <--
1: Enable secure boot by pin strap
(4)Enable Low Security Secure Boot Key by Pin Strap (FWSPIMISO) <--HW setting
0: Disable <--
1: Enable Low Security Secure Boot Key by Pin Strap

When SCU510[30]=1 <--SW setting
Boot SPI Flash size bit[15 14 13]) (OTPSTRAP[47:45])
000: no de?ne size (default)
001: 2MB
010: 4MB
011: 8MB
100: 16MB
101: 32MB
110: 64MB
111: 128MB
Host SPI Flash size bit[21 20 19]
000: no de?ne size (default)
001: 2MB
010: 4MB
011: 8MB
100: 16MB
101: 32MB
Host SPI CRTM size (trap hspi crtmsize[26 25]) (OTPSTRAP[58:57])
00: disable CRTM (default)
01: 1MB
10: 2MB
11: 4MB
110: 64MB
111: 128MB
Enable Secure Boot by Pin Strap (FWSPIMOSI)
0: Disable
1: Enable secure boot by pin strap
Enable Low Security Secure Boot Key by Pin Strap (FWSPIMISO)
0: Disable
1: Enable Low Security Secure Boot Key by Pin Strap




I2C Address: 1001000=0X48




### 1.3.3 Hardware strap configuration method

- TXD5: embedded internal pull high resistor of value 26K ~ 71K.
  Please add external 10k ohm pull-up for A0 chip.
  - Strap value = 0, just leave the pin floating or pull up.
  - Strap value = 1, pull-down the pin to ground by a resistor of value 1K ~ 4.7K Ω.
- FWSPICK, FWSPIMOSI, FWSPIMISO: embedded internal pull low of value 33K ~ 89K
  - Strap value = 0, just leave the pin floating.
  - Strap value = 1, pull-high the pin to 3.3V standby power by a resistor of value 1K ~ 4.7K Ω.
- GPIOY[5:4], GPIOZ[7:3]: embedded internal pull low of value 33K ~ 89K
  - Strap value = 0, just leave the pin floating.
  - Strap value = 1, pull-high the pin to 3.3V standby power by a resistor of value 1K ~ 4.7K Ω.

### 1.3.1 Method 1: Load from dedicated strap pins

**Strap function pins when SCU510[30]=0**

There are 5 dedicated strap function pins when SCU510[30]=0. Listed as below:

| | | | |
|---|---|---|---|
| TXD5* | SCU500[0] | Disable ARM CA7 CPU boot | |
| GPIOZ4 | SCU510[6] | Select LPC/eSPI (Need Firmware) | (or with OTPSTRAP[38]) |
| FWSPICK | SCU510[8] | Enable Boot from Uart5 | |
| FWSPIMOSI | SCU510[31] | Enable Secure Boot by Pin Strap | |
| FWSPIMISO | SCU51C[0] | Enable Low Secure Boot function | |

**Strap function pins when SCU510[30]=1**

There are 11 dedicated strap function pins when SCU510[30]=1. Listed as below:

| | | | |
|---|---|---|---|
| TXD5* | SCU500[0] | Disable ARM CA7 CPU boot | |
| GPIOZ6 | SCU510[13] | Boot SPI flash size Bit [0] | (replace OTPSTRAP[45]) |
| GPIOZ7 | SCU510[14] | Boot SPI flash size Bit [1] | (replace OTPSTRAP[46]) |
| FWSPICK | SCU510[15] | Boot SPI flash size Bit [2] | (replace OTPSTRAP[47]) |
| GPIOZ3 | SCU510[19] | Host SPI flash size Bit [0] | (replace OTPSTRAP[51]) |
| GPIOZ4 | SCU510[20] | Host SPI flash size Bit [1] | (replace OTPSTRAP[52]) |
| GPIOZ5 | SCU510[21] | Host SPI flash size Bit [2] | (replace OTPSTRAP[53]) |
| GPIOY4 | SCU510[25] | Host SPI CRTM size Bit [0] | (replace OTPSTRAP[57]) |
| GPIOY5 | SCU510[26] | Host SPI CRTM size Bit [1] | (replace OTPSTRAP[58]) |
| FWSPIMOSI | SCU510[31] | Enable Secure Boot by Pin Strap | |
| FWSPIMISO | SCU51C[0] | Enable Low Secure Boot function | |

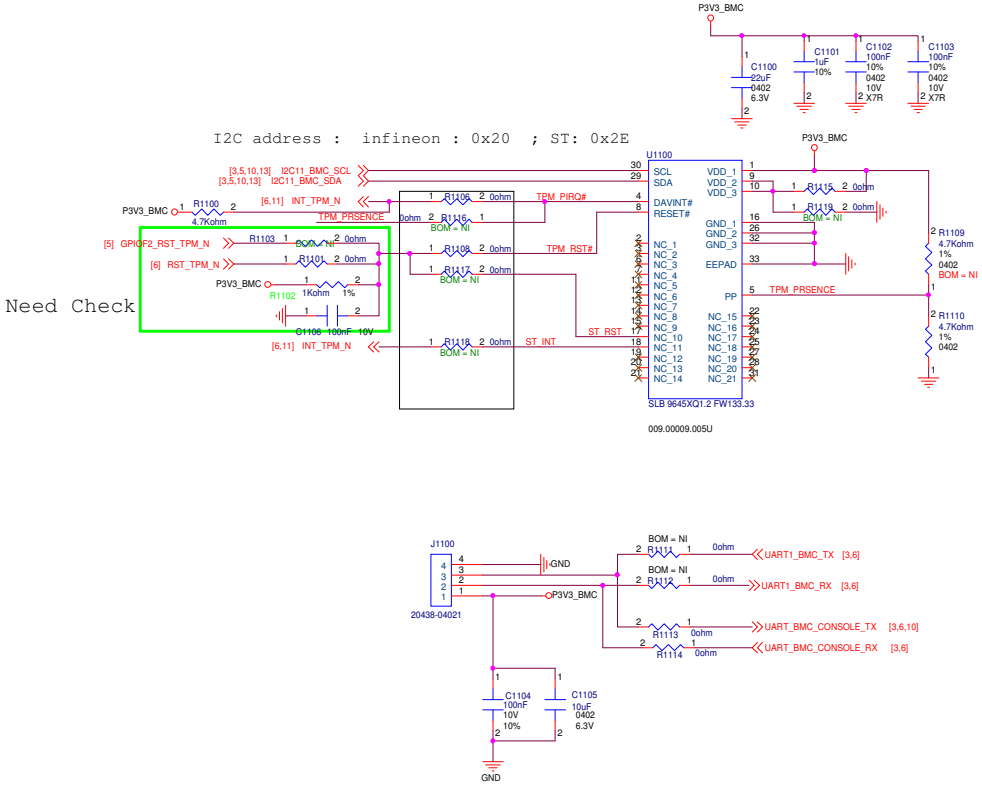
Intel Confidential

# BMC_AST2600_HW_STRAPPING

<Variant Name>

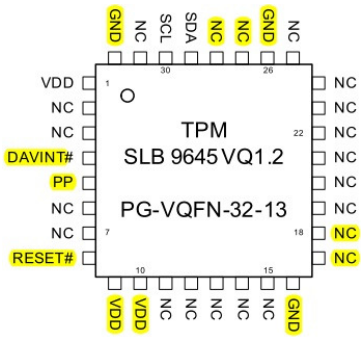
| | |
|---|---|
| SWITCH R&D CENTER | CONFIDENTIAL |
| Title: S9501 Series BMC Card | |
| Size: C | Document Number: Project: T77O994T03 |
| Rev: 00 X A1 | |
| Date: 19:39:16 Thursday, October 29, 2020 | Sheet 10 of 18 |

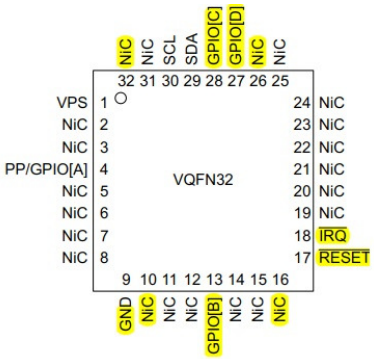
# TPM










Infineon:
mount
INT:R1106
Reset: R1108
VDD:R1115
unmount : R1116 R1117 R1118 R1119
ST: 009.00011.005 ;ST33HTPH2E32AHC2
mount
INT:R1118
Reset: R1117
Gnd:R1119
unmount : R1106 R1108 R1115

<Variant Name>

| SWITCH R&D CENTER | CONFIDENTIAL |
|---|---|
| Title: S9501 Series BMC Card | |
| Size: C | Document Number: T77O994T03 / Project: | Rev: 00 X A1 |
| Date: 19:39:16 Thursday, October 29, 2020 | Sheet 11 of 18 |

[3,7] BMC_PWM6 >> BMC_FAN_PWM6 [3,7]

[3,7] BMC_PWM1 >> BMC_FAN_PWM1 [3,7]

[3,7] BMC_PWM2 >> BMC_FAN_PWM2 [3,7]

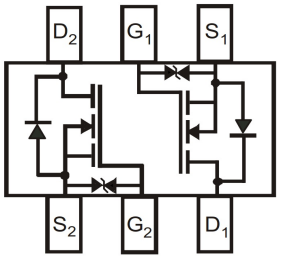
[3,7] BMC_PWM3 >> BMC_FAN_PWM3 [3,7]

[3,7] BMC_PWM4 >> BMC_FAN_PWM4 [3,7]

[3,7] BMC_PWM5 >> BMC_FAN_PWM5 [3,7]

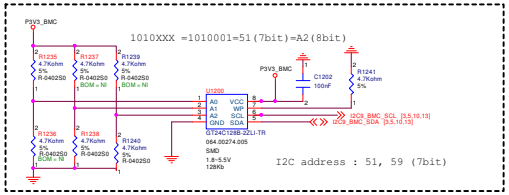
[3,7] BMC_PWM6 >> BMC_FAN_PWM6 [3,7]

[3,7] BMC_PWM7 >> BMC_FAN_PWM7 [3,7]




Top View
Internal Schematic

FRU




```
Write Protect: Connecting the WP pin to GND
will ensure normal write operations.When the WP
pin is connected to VCC, all write operations
to the memory are inhibited.
```

| FRU | Description | Location | I2C BUS | I2C address |
|---|---|---|---|---|
| I2C Identification EEPROM. Identification field can be programmed in "M/B Custom Field 1" | EEPROM used for FRU data, system purposes, identification. Motherboard designers should allow access for the HOST SMBus to access identification FRU on I2C BUS 9. | RunBMC module | 9 | 0xA2, 8bit |
| I2C Personality EEPROM | EEPROM used by SOC to define personality of system | System Board | 4 | 0xA0, 8bit |

Table 37 RunBMC FRU Requirements

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | 1 | 0 | 1 | 0 | A2 | A1 | A0 | R/$\overline{W}$ |

<Variant Name>

| SWITCH R&D CENTER | CONFIDENTIAL |
|---|---|

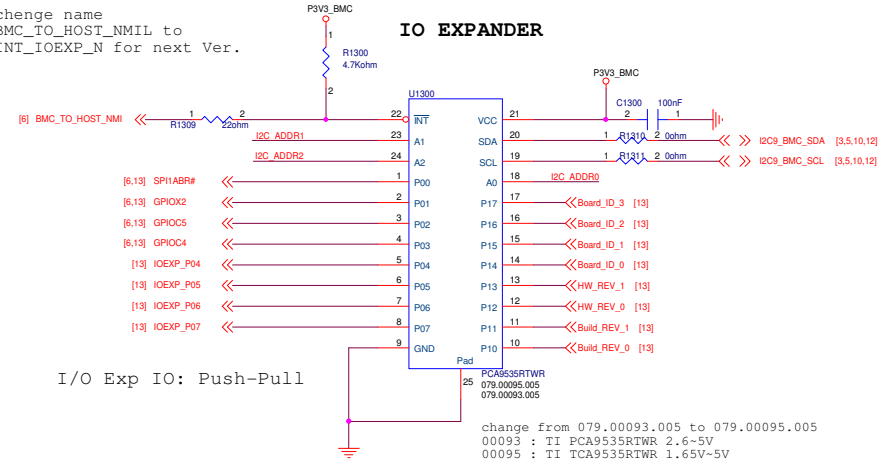
Title: S9501 Series BMC Card

| Size | Document Number | Rev |
|---|---|---|
| D | Project: T77O994T03 | 00 X A1 |

Date: 19:59:17 Thursday, October 29, 2020 Sheet 12 of 18

chenge name
BMC_TO_HOST_NMIL to
INT_IOEXP_N for next Ver.

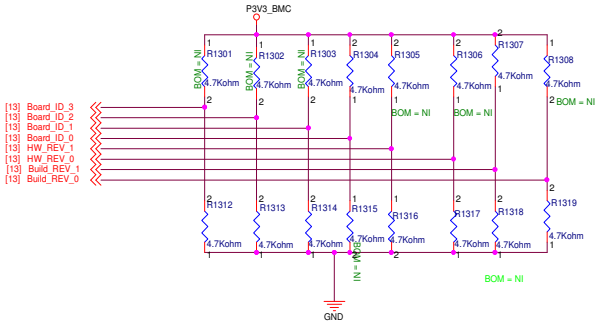
## IO EXPANDER




I/O Exp IO: Push-Pull

change from 079.00093.005 to 079.00095.005
00093 : TI PCA9535RTWR 2.6~5V
00095 : TI TCA9535RTWR 1.65V~5V

## 0 0 0 1  00  1 0

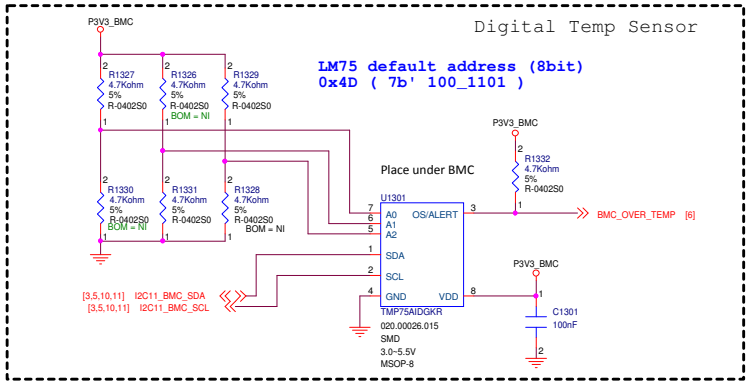


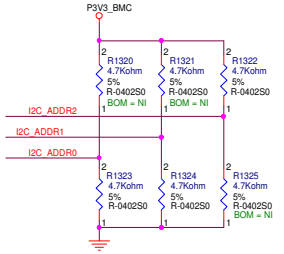

Board ID [3:0]:
0000: Dummy BMC
0001: Aspeed BMC
0010: NXP BMC
0011~1111: Reserved

Hardware Revision [1:0]:
Proto : 00
Alpha : 01
Beta : 10
PVT : 11

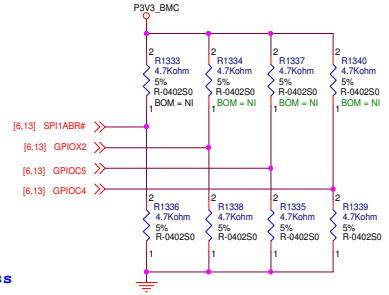
Build Rev [1:0]:
A1 : 00
A2 : 01
A3 : 10
A4 : 11

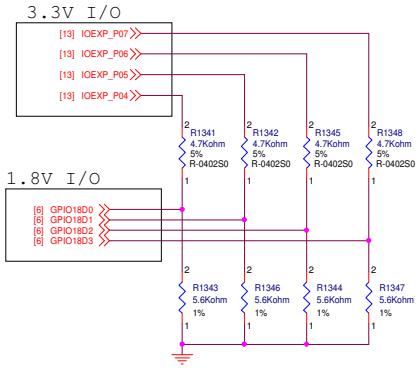
## Digital Temp Sensor



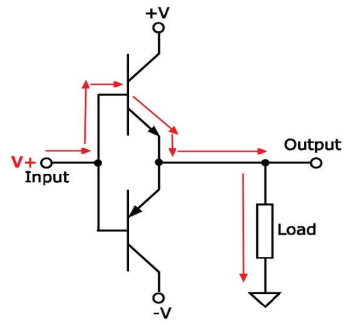




PCA9535 default address
0x24 ( 7b' 010_0100 )



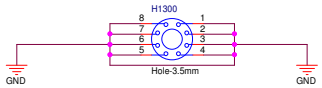




1 K: 1.21K =1.807V
4.7K:5.6K=1.794V
3.24K:3.9K:=1.802521
10K:12K=1.8V




## MOUNTING HOLE

Mounting Hole = 3.5mm

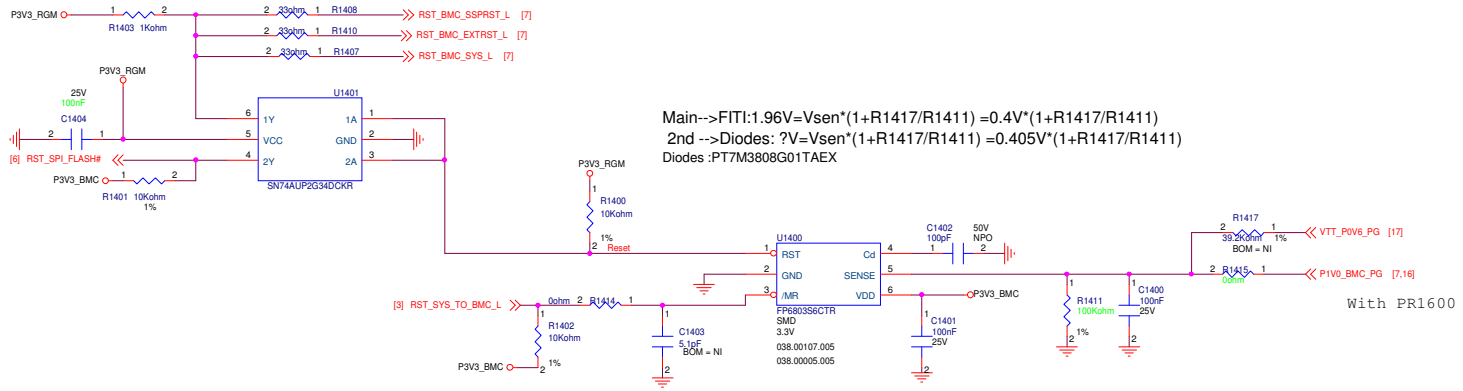


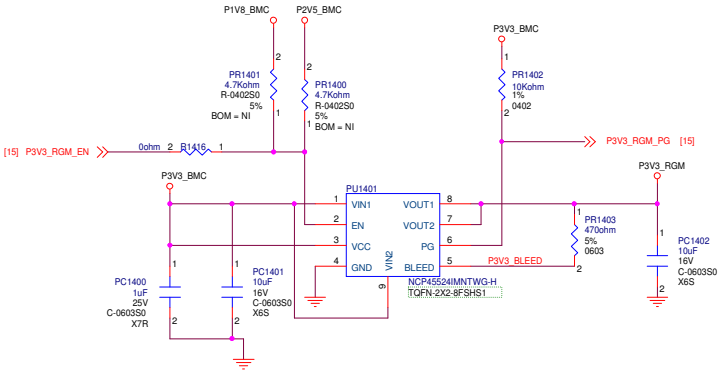

LABEL1300
503.01043.005
LABEL

PCB1300
309.00203.005
Plated Gold : 0.254um
PCB

<Variant Name>

| SWITCH R&D CENTER | CONFIDENTIAL |
|---|---|
| Title: S9501 Series BMC Card | |
| Size: C | Document Number / Project: T77O994T03 — Rev: 00 X A1 |
| Date: 19:39:17 Thursday, October 29, 2020 | Sheet 13 of 18 |




# BMC_PWR RESET

<Variant Name>

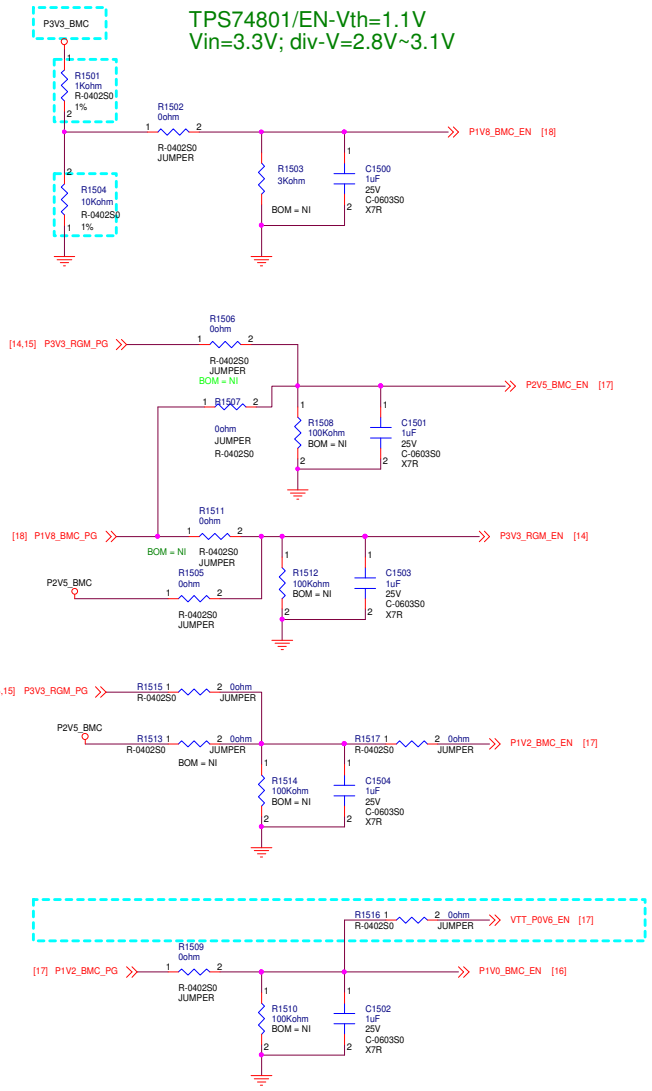
| SWITCH R&D CENTER | CONFIDENTIAL |
|---|---|

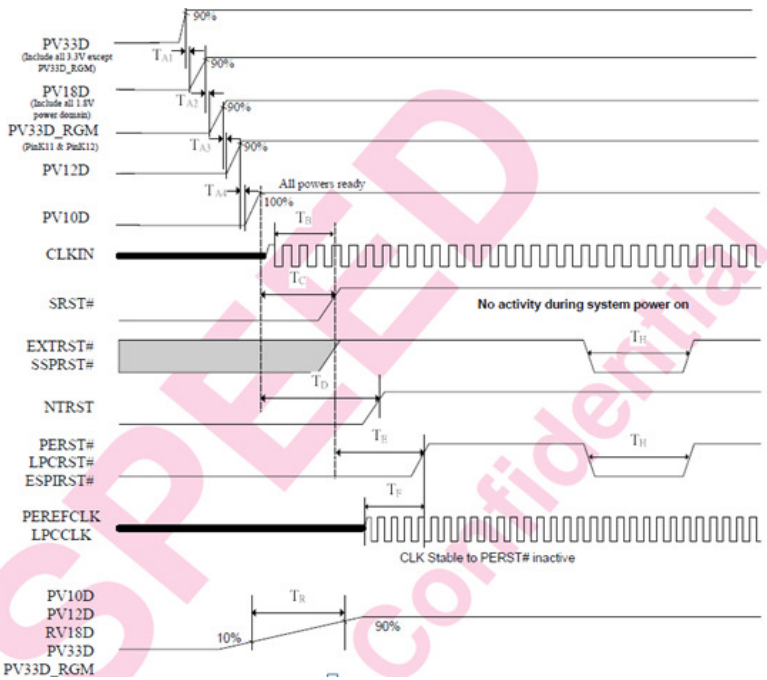
Title: S9501 Series BMC Card

| Size | Document Number | Rev |
|---|---|---|
| C | Project: T77O994T03 | 00 X A1 |

Date: 19:39:17 Thursday, October 29, 2020 Sheet 14 of 18

# BMC Power up Sequence




P2V5 must be equal or greater than P1V2 at all times for DDR4

SPEED Confidential

<Variant Name>

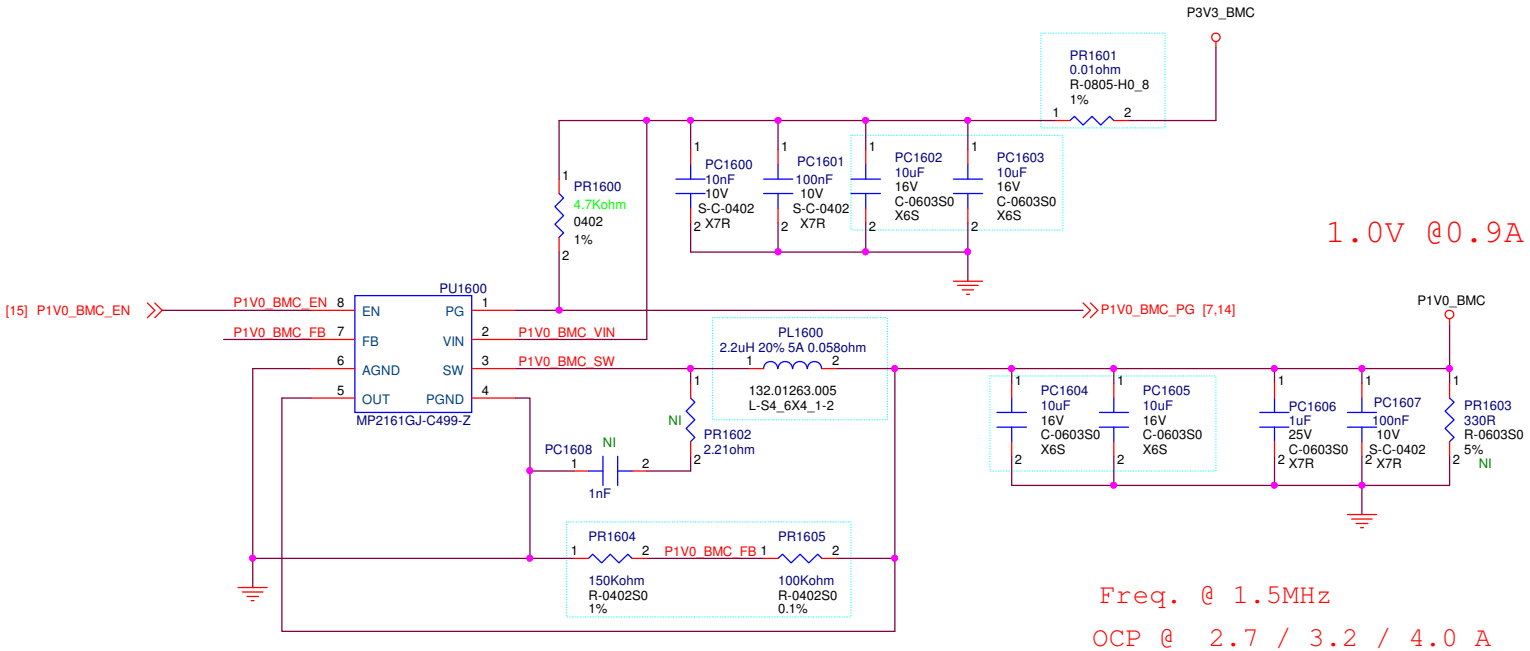
| SWITCH R&D CENTER | CONFIDENTIAL |
|---|---|

Title: S9501 Series BMC Card

| Size | Document Number | Rev |
|---|---|---|
| C | Project: T77O994T03 | 00 X A1 |

Date: 19:39:16 Thursday, October 29, 2020 Sheet 15 of 18

# P1V0_0.9A

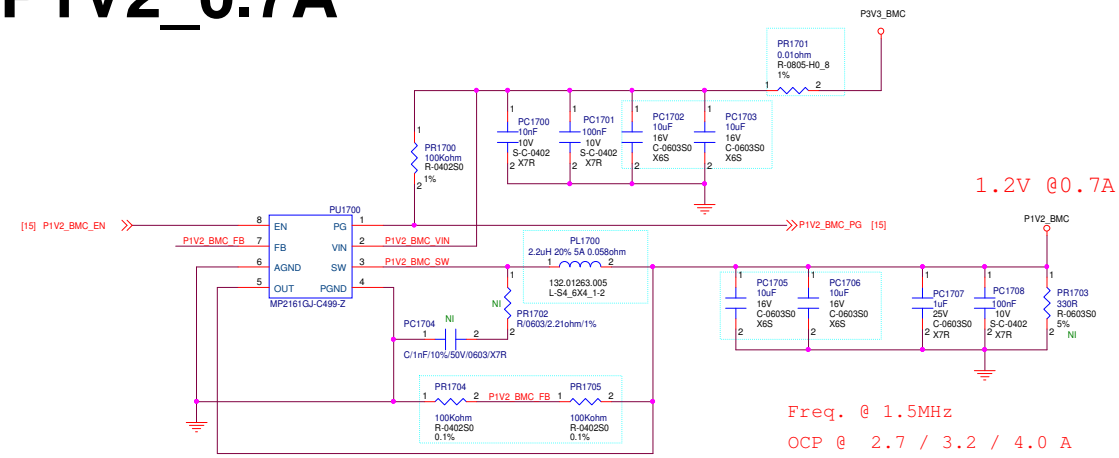



## *3.3V to 1V0_BMC/0.9A*

<Variant Name>

| SWITCH R&D CENTER | CONFIDENTIAL |
|---|---|
| Title: S9501 Series BMC Card | |
| Size: B | Document Number: Project: T77O994T03 — Rev: 00 X A1 |
| Date: 19:39:16 Thursday, October 29, 2020 | Sheet 16 of 18 |

# P1V2_0.7A




1.2V @0.7A

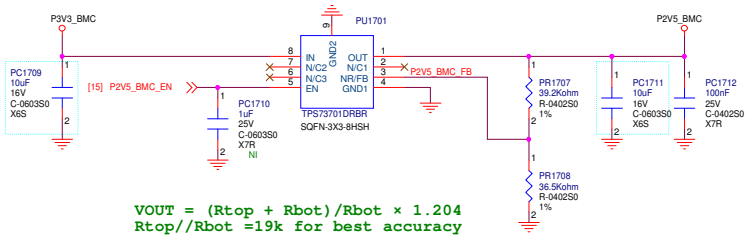
Freq. @ 1.5MHz

OCP @ 2.7 / 3.2 / 4.0 A

Soft-Start:1.5mS

Vo=0.6*(1+PR1705/PR1704)=1.2V

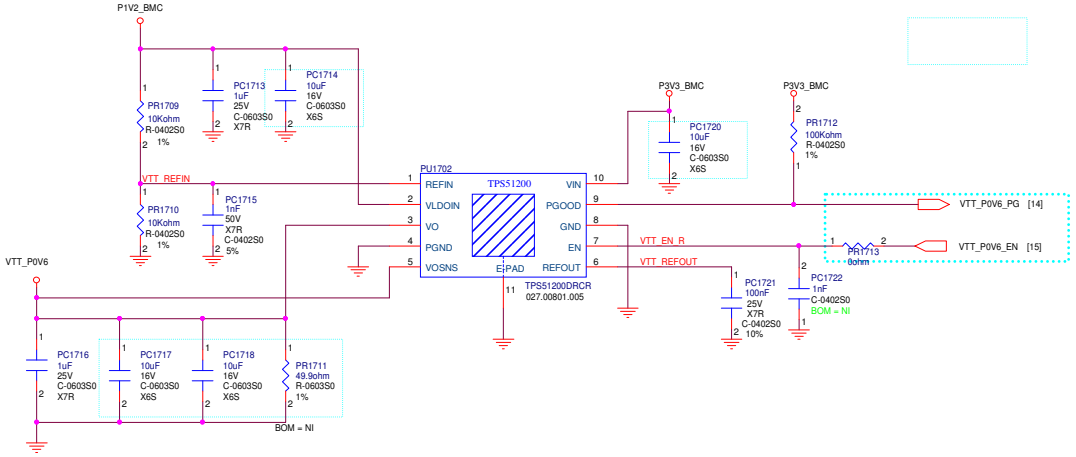
## 3.3V to 2V5_BMC/0.02A




VOUT = (Rtop + Rbot)/Rbot × 1.204

Rtop//Rbot =19k for best accuracy

## 3.3V to 1V2_BMC/0.7A




## *1.2V to 0.6V_DDR4_VTT / TPS51200 @ 0.25A*

<Variant Name>

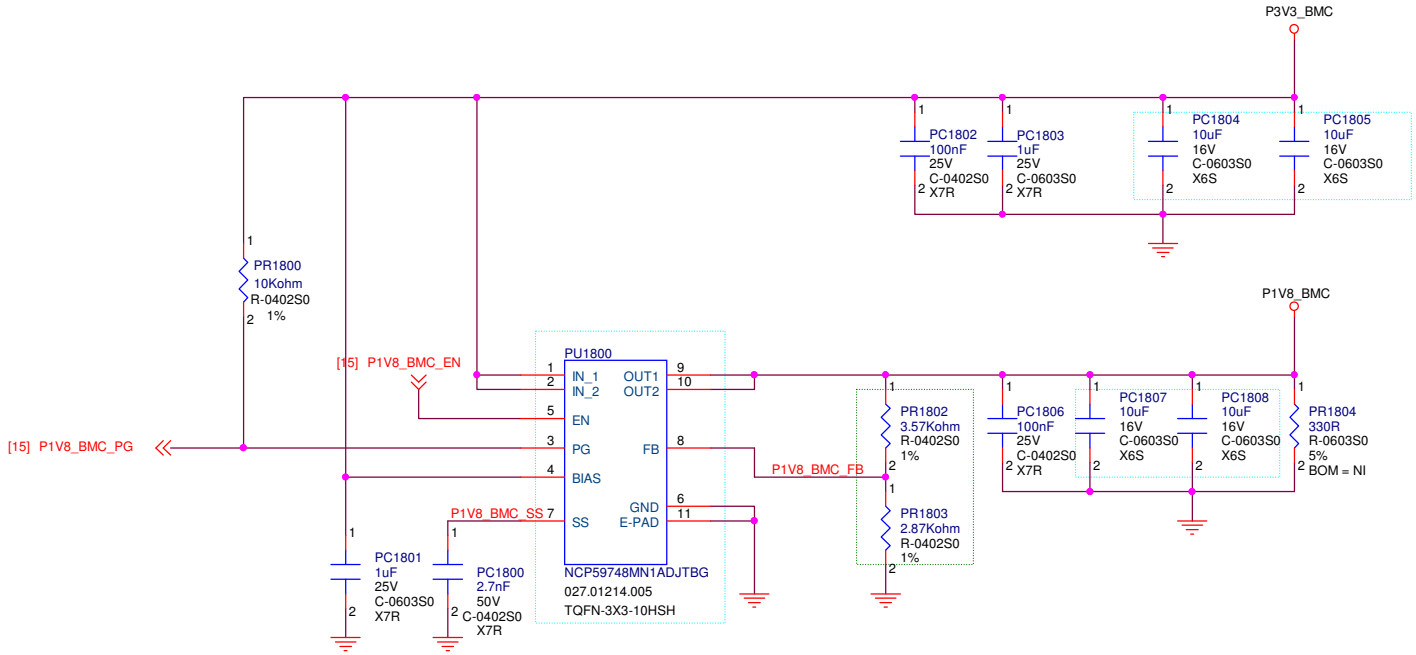
| SWITCH R&D CENTER | CONFIDENTIAL |
|---|---|

Title: S9501 Series BMC Card

| Size | Document Number | Rev |
|---|---|---|
| C | Project: T77O994T03 | 00 X A1 |

Date: 19:39:16 Thursday, October 29, 2020 Sheet 17 of 18

# P1V8_0.31A




027.01214.005 with 027.00808.005 pin to pin

**Vo=0.8*(1+PR1802/PR1803)=1.8V**

**Soft-start Time : 5ms**

## *3.3V to 1V8_BMC/0.31A*

<Variant Name>

| SWITCH R&D CENTER | CONFIDENTIAL |
|---|---|
| Title: S9501 Series BMC Card | |
| Size: B | Document Number: Project: T77O994T03 — Rev: 00 X A1 |
| Date: 19:39:16 Thursday, October 29, 2020 | Sheet 18 of 18 |